

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

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Alok Jain, et al.FILING DATE
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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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W	S. Kundu, "GateMaker: A Transistor to Gate Level Model Extractor for Simulation, Automatic Test Pattern Generation and Verification," International Test Conference, pp. 372-381, 1998.
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W	R. E. Bryant, "Boolean Analysis of MOS Circuits," IEEE Transactions on Computer Aided Design, pp. 634-649, July 1987.
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EXAMINER	DATE CONSIDERED
2004	7/2004

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